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(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 718 881 A2

# (12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
**26.06.1996 Bulletin 1996/26**

(51) Int Cl.[6]: **H01L 21/765**, H01L 27/118

(21) Application number: **95308542.0**

(22) Date of filing: **28.11.1995**

(84) Designated Contracting States:
**DE FR GB IT**

(30) Priority: **20.12.1994 US 360978**

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## (54) Isolation by active transistors with grounded gates

(57) An isolation gate structure is formed between active areas on a P-type semiconductor substrate. The isolation structure includes a thick gate oxide layer over which is formed a P-doped polycrystalline silicon layer. The polycrystalline silicon layer is electrically connected to the substrate, by buried contact if desired, and can further be electrically connected to a source region formed within the active area. The polycrystalline silicon layer and substrate are connected to ground potential, thus preventing current flow between active areas.

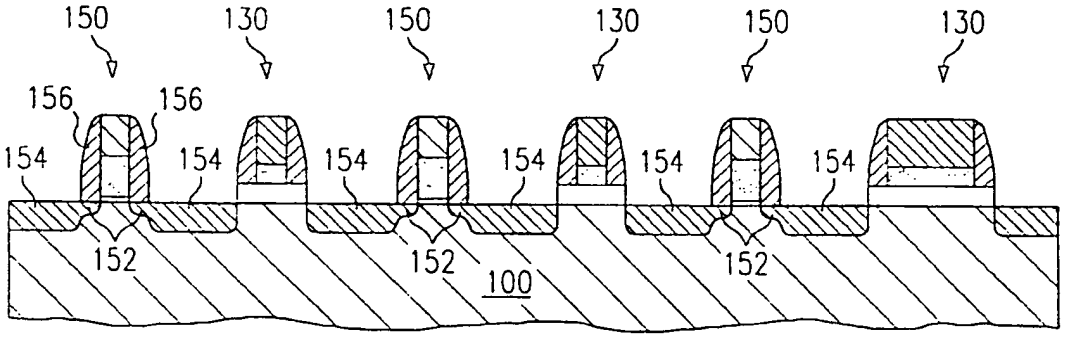


*FIG. 9*

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## Description

This invention relates generally to integrated electronic circuits, and more particularly to isolation of active regions in MOS integrated circuits.

In today's metal-oxide semiconductor (MOS) integrated circuit design, active regions on a chip are isolated from each other by a thick layer of thermally grown oxide, known as a field oxide, overlying doped channel-stop regions. This method of isolation has a number of disadvantages that become increasingly apparent with higher component density on the chip. The field oxide grows in areas not covered by a nitride mask layer used to define the active regions during processing. The use of a nitride mask forms a characteristic "bird's beak" shape in the oxide that consumes what would otherwise be usable active area while insignificantly contributing to the isolation function of the field oxide. The channel-stop dopants may also diffuse into the active area upon thermal growth of the field oxide, causing a narrow channel effect and increasing required threshold voltages for components constructed in the active regions. Further, mobile ions arising from electrical stress can cause shifts in the field threshold voltage, resulting in inconsistent performance of active circuit components.

In an isolation structure known as the "sea-of-gates," every other one of transistors has a grounded gate, thereby isolating those transistors without grounded gates on each of two opposite sides, while the traditional field oxide and channel stops are used to complete the isolation. However, all of the transistors in "sea-of-gate" design are of identical construction, and those with grounded gates are not therefore expressly designed or tailored for the isolation function they serve.

With increasing component density in today's integrated circuit design, it is highly desirable to provide effective isolation of active regions on a chip while minimizing the consumption of otherwise usable active area unnecessary to the isolation function.

According to the present invention, an isolation gate structure is constructed between or around active areas of a semiconductor substrate by forming an insulating layer on the surface of the substrate, forming a polycrystalline silicon layer on the insulating layer, and selectively etching away portions of the deposited layers to expose the active areas of the semiconductor substrate for further processing. The polycrystalline silicon layer is preferably of the same conductivity type as the substrate and is regularly connected to the substrate at buried contacts, thereby ensuring that the polycrystalline silicon layer and substrate remain at the same electric potential. The polycrystalline silicon layer is connected to a constant value electric potential supply selected to prevent current flow between active areas. Further, the polycrystalline silicon layer can be connected to a source or drain region of the active area, as appropriate, with metal or metal silicide local interconnects .

Figure 1 is a cross-sectional view showing the prior art isolation of active areas by a thick layer of field oxide exhibiting the characteristic bird's beak.

Figure 2 shows a cross-sectional view of a portion of P-type substrate upon which an integrated circuit structure according to the present invention is to be formed.

Figure 3 is a view of layers grown and deposited according to the present invention on the surface of the substrate of Figure 2.

Figure 4 shows a selective etching of the layers of Figure 3.

Figure 5 is a top view of the selectively etched layers of Figure 4, showing one possible embodiment of a circuit structure.

Figure 6 shows an oxide layer deposited on top of the selectively etched layers of Figure 4.

Figure 7 shows a selective etching of the layers of Figure 6 and subsequently grown and deposited layers.

Figure 8 shows a selective etching of the layers of Figure 7 and a subsequent N-type implant preparatory to configuration of lightly doped drain and source structures.

Figure 9 shows the layers of Figure 8 with the addition of oxide side spacers and implanted drain and source regions.

Figure 10 is an electrical schematic diagram of the structure of Figure 9, showing electrical connections to ground potential.

Figure 11 is a top view of Figure 9, showing one possible embodiment of a circuit structure, and showing electrical connections to ground potential schematically.

Figure 12 is a top view showing a second possible embodiment of a circuit structure.

Figure 1 shows the NMOS prior art isolation of active areas 108 in a P-type substrate 100 by a thick layer of thermally grown field oxide 102. Below the field oxide 102 are channel-stop regions 104 formed by P-type implants which diffuse into the substrate 100 upon the thermal growth of the field oxide. The shape of the field oxide 102 exhibits the characteristic bird's beak feature 106 that arises from the field oxide penetrating beneath a silicon nitride layer used to define the active areas 108 on the chip during field oxide growth. One drawback of the current art method of forming the field oxide 102 is that if the active area 108 dimensions are too small, bird's beak encroachment can lift up and separate the silicon nitride layer from the underlying silicon, resulting in an even longer bird's beak structure or possible loss of all active area.

The bird's beak 106 is unnecessary to the isolating function of the field oxide 102 and disadvantageously consumes what would otherwise be active area of the substrate 100 usable for circuit component construction. In current art integrated circuit construction, each bird's beak 106 can extend, in some designs, in excess of 2500 angstroms into what would otherwise be usable active area. Additionally, the doped channel-stop regions 104 diffuse into the active areas and in some de-

signs may cause a narrow channel effect, raising the threshold voltage of transistors constructed in the active areas. The bird's beak feature 106 of the field oxide 102, as well as the narrow channel effect produced by the channel-stop region 104, limits both the minimum dimensions separating active areas 108 and the minimum size of those active areas, thus causing difficulties in increasing the integration density. As seen in Figure 9, and as discussed in detail below, practice of the present invention accomplishes the desired isolation with a minimum spacing between active areas of the substrate 100.

Figures 2-9 illustrate the main steps carried out in practicing the present invention and the structure of the present invention. Figure 2 shows a semiconductor substrate 100 which, in accordance with the present invention, is preferably doped either N-type or P-type. The substrate 100 could be substrate itself or, alternatively, an N-well or P-well used in connection with a CMOS process, a doped epitaxial layer, or other substrate structure. In one embodiment, the substrate 100 is doped with Boron in approximate concentration of $10^{16}$-$10^{17}/cm^3$. Additional processing steps such as threshold adjustment implants, epitaxial growth, well formation and the like may be carried out as desired for each design. While the main steps according to the present invention are shown and described herein, every single step in the entire process need not be shown because such are part of the standard processing steps commonly used and known in the art.

Referring to Figure 3, a first gate insulator layer or oxide 120 is grown over the entire substrate 100, followed by a deposited first polycrystalline silicon layer 122 and a deposited covering oxide layer 124. In the preferred embodiment, the first gate oxide layer 120 is somewhat thicker than a gate oxide layer used for an active transistor on the same chip. For example, the first gate oxide layer 120 may be approximately 500 angstroms thick if the standard gate oxide layer thickness is in the range of 90-200 angstroms. This ensures a slightly higher threshold voltage for the isolation gate structure 130 to be formed (see Figure 4). In the preferred embodiment, the polysilicon layer 122 is in the range of 500 angstroms thick, but could be somewhat more or less as desired. The deposited oxide layer 124 is approximately 2000 angstroms thick. In the embodiment with a P-type substrate 100, the first polycrystalline layer is preferably doped with a P-type impurity such as Boron and in concentration roughly two to five times that of the substrate. The doping concentration of the first polysilicon layer 122 is selected to provide adequate conductivity but not be so high that Boron atoms migrate into the substrate 100 in sufficient quantity to affect the conductivity of the substrate. The slightly thicker oxide 120 also helps prevent this migration.

In the preferred embodiment, the polysilicon 122 is doped with the same conductivity type as the substrate This provides the advantage that direct ohmic contact via a buried contact to the substrate is possible. This also reduces the risk of problems if there is a pin-hole in the oxide with some slight migration of ions. Thus, on an N-type substrate, the first polysilicon layer is doped N-type. The oxide layer may be made thinner or thicker, depending on the dopant ions used and the concentrations thereof, since some ions have a lesser tendency to migrate than others.

Referring to Figures 4 and 5, the surface of the chip is patterned and etched to form an isolation gate structure 130. As best seen in Figure 5, one possible circuit configuration has the isolation gate structure 130 surrounding each of active regions 108 in which transistor structures will be formed by subsequent processing steps. In the case of a P-type substrate 100, the first polycrystalline layer 122 is preferably electrically connected to the lowest voltage supplied to the chip, typically ground potential, to ensure that the region 132 under the isolation gate 130 never conducts, thereby electrically isolating regions 108 from one another. Most often, the substrate 100 will also be connected to this lowest voltage, and in such structures it is advantageous to provide regular and direct contact between the first polycrystalline layer 122 and the substrate, by metallization layers and/or buried contacts, not shown because such are well known in the art, and any suitable ohmic layer contact to the substrate is acceptable.

The comparable doping of the substrate 100 and the first polycrystalline layer 122 provides for an ohmic connection at the buried contacts, and renders harmless any diffusion effects arising from pin-hole defects in the oxide layer 120. A further advantage is that the grounded isolation gate structure 130 will shield against any field threshold shifts arising from mobile ions. It will be appreciated that the greatest advantage of tthe present invention is achieving the function of isolation with minimal dimension requirements. The isolation structure 130 of the present invention requires only the current art minimum dimensions for forming a gate structure as opposed to the in excess of three times larger minimum dimensions required for current art isolation field oxide growth.

The first gate oxide layer 120 is preferably somewhat thicker than an oxide layer for an operating transistor of the same circuit, resulting in a relatively higher magnitude threshold voltage to turn on the "channel" region 132 under the isolation gate 130. Indeed, turning on the "channel" region 132 is neither anticipated nor desired. In the case of a P-type substrate 100, the grounding of the first polycrystalline silicon layer 122 to the lowest voltage on the chip and the thick gate oxide 120 are design features tailoring the gate 130 for isolation purposes and keeping this "channel" region 132 turned off to perform the isolation. The same conductivity type doping permits easy grounding of the polysilicon 122 to the substrate 100 if desired. Of course, the isolation method and structure of the invention are applicable to a thin gate oxide 120 if design permits, the ob-

ject being to prevent deleterious migration of dopant between the poly layer 122 and the substrate 100 and to keep the "channel" 132 off at all times

In the next process step, an oxide (LTO) layer 134 is formed over the entire chip (see Figure 6) by any acceptable technique, by growth or preferably using a chemical vapor deposition (CVD) process. Referring to Figure 7, the oxide layer 134 is then etched using an anisotropic plasma etch, resulting in sidewall spacers 136 alongside the isolation gate structure 130. Both the sidewall spacers 136 and the covering oxide layer 124 guard against the short circuiting of the isolation gate structure 130 with other constructed circuit components. The covering oxide layer 124 also guards against contamination of the doped first polycrystalline silicon layer 122 by subsequent ion implantation procedures.

The exposed portion of the first gate oxide layer 120 is removed and a second gate oxide 140, with preferable thickness in the range of approximately 90-120 angstroms, is grown in its place. A second polycrystalline silicon layer 142, of approximately 1500 angstroms thickness, is then deposited over the surface of the chip, and subsequently a titanium silicide or other metal silicide layer 144, also of approximately 1500 angstroms thickness, is deposited. In the case of a P-type substrate 100, the covering oxide layer 124 prevents the Boron dopant in the first polycrystalline silicon layer 122 from migrating into the second polycrystalline silicon layer 142 which is itself negatively doped for lower resistivity.

Referring to Figure 8, the surface of the chip is patterned and etched to form gate structures 150. Implants are made to form lightly doped drain (LDD) and source extensions 152. After LDD implant and anneal, and as seen in Figure 9, sidewall spacers 156 are formed on the gate structures 150 by anisotropic etch of a CVD oxide layer. Heavily doped drain and source regions 154 are then formed by ion implantation and anneal as is well known in the art. Subsequent processing and finishing steps are well known to the art, such as a further CVD layers with contact holes for metallization overlays and a finishing overglass layer, and are neither further described nor depicted in the figures.

Figure 11 is a top view of Figure 9, showing one possible embodiment of a circuit structure incorporating the present invention, and indicates the gate, source and drain portions of the active regions 108 surrounded and separated by the isolation gate structure 130. A connection of the isolation gate 130 to ground, by buried contact to the P-type substrate 100, is shown schematically at 158. Buried contacts between the first poly layer 122 and the substrate 100 are formed at regular intervals and with proper spacing to ensure good ohmic electrical contact between the first polysilicon and the substrate, and to ensure the equipotential nature of the first poly and substrate. Of course, this type of structure is repeated throughout the chip and only a portion of the chip is shown. Active areas 108 will be formed above and below those shown in Figure 11, and all the active areas are isolated by the gate isolation structure 130 in those places where field oxide was previously used.

Figure 12 is a top view showing a second possible embodiment of a circuit configuration where the isolation gate structure 130 is formed between, but does not surround, active areas 108. Indeed, as is common in the art, two such adjacent active areas 108 may be contiguous at, for example, a common source region (not shown). The isolation gate structure 130 isolates these active areas 108, just as current art field oxide does in such circuit designs, but advantageously allows the active regions 108 to be spaced more closely.

Figure 10 is a schematic diagram of the structure of Figure 9, showing electrical connections to ground potential of a source 160, the substrate 100 and the isolation gate structure 130. Many circuits have the source and substrate connected to the same low voltage potential, usually ground. Both the substrate 100 and isolation gate structure 130 are tied to the same voltage potential as the grounded source 160. Should it be desirable, the grounded source 160 can also be electrically connected to the substrate 100 via metal or metal silicide local interconnects as is common in the art. Further, the isolation gate structure 130 can be electrically connected to the grounded source 160 by metal or metal silicide local interconnects as desired. If a contact is made between the isolation gate 130 and the source 160, a metal contact of some type is preferred to ensure a PN junction is not formed because the source 160 and the poly of the isolation structure 130 would usually be of opposite conductivity types.

It will be appreciated that, while an illustrative embodiment of the invention has been described for purposes of illustration, modifications may be made without departing from the spirit and scope of the invention. For example, the order of process operations could be changed so as to construct the isolation gate structure from the second poly layer after the circuit component gates have been formed. The specific details for the construction of an isolation gate structure over a P-type substrate for isolating N-channel field-effect enhancement mode transistors has been described above. However, it will be appreciated by those skilled in the art that the present invention can be applied to a wide range of MOS integrated circuit structures to replace the field oxide isolation structure. As one example, a reversal of conductivity types allows a similar isolation gate structure to be formed in an N-type substrate. In this embodiment, the poly silicon 122 is doped N-type and is tied to the highest voltage potential on the chip, usually the N well, to ensure that the region of the substrate underlying the isolation gate structure never conducts and always isolates the active areas in the N-type substrate from each other.

The invention may also be used on the same chip in combination with field oxide isolation. For example, the isolation gate structure may be used within a memory array where space is precious and standard field

oxide isolation can be used in the peripheral circuits, as desired.

While various embodiments have been described in this application for illustrative purposes, the claims are not limited to these embodiments. Many modifications can be made to the structures and methods shown and described herein that take advantage of the present invention. For example, some method steps can be added or substituted for the steps disclosed and claimed herein to achieve this invention

**Claims**

1. An isolating structure for an integrated circuit, comprising:

   a first region of a first conductivity type in a semiconductor substrate;

   second and third regions of a second conductivity type in said substrate, said first region being disposed between said second and third regions;

   an insulator layer overlying said first region;

   a polycrystalline silicon layer overlying said insulator layer;

   a constant value electric potential supply; and

   an electrical contact between said polycrystalline silicon layer and said constant value electric potential supply, the value of said electric potential being selected to prevent current flow between said second and third regions to electrically isolate them from each other.

2. The isolating structure described in claim 1 wherein said polycrystalline silicon layer is of said first conductivity type, said insulator layer has an opening to said substrate, and said polycrystalline silicon layer fills said opening and contacts said substrate to provide an ohmic contact between said polycrystalline silicon layer and said substrate.

3. The isolating structure described in claim 1 wherein said polycrystalline silicon layer is electrically connected to said second region either by a metal electrical connection or by a metal silicide local interconnect.

4. The isolating structure described in claim 1 wherein said polycrystalline silicon layer has a doping concentration approximately two to five times a doping concentration of said substrate.

5. An isolating structure for an integrated circuit, comprising:

   a semiconductor substrate having an active area and an isolation area surrounding said active area;

   an insulation layer overlying said isolation area and surrounding said active area.

   a polycrystalline silicon layer overlying said insulating layer and surrounding said active area;

   a constant value electric potential supply; and

   an electrical connection between said polycrystalline silicon layer and said constant value electric potential supply, the value of said electric potential being selected to ensure that said isolation area underlying said insulating layer is prevented from conducting electric currents therein.

6. The isolation structure described in claim 5 wherein said semiconductor substrate is of P-type, and wherein said selected electric potential is either ground potential or a lowest electric potential supplied to the integrated circuit.

7. The isolation structure described in claim 5 wherein said semiconductor substrate is of N-type, and wherein said selected electric potential is a highest electric potential supplied to the integrated circuit.

8. The isolation structure described in claim 5 wherein said semiconductor substrate is of P-type, said active area includes a field-effect transistor having a source, and further including an ohmic interconnection between said polycrystalline silicon layer and said source for ensuring that an electric potential of said polycrystalline silicon layer does not exceed an electric potential of said source.

9. The isolation structure described in claim 5 wherein said semiconductor substrate is of N-type, said active area includes a field-effect transistor having a drain, and further including an ohmic interconnection between said polycrystalline silicon layer and said drain for ensuring that an electric potential of said drain does not exceed an electric potential of said polycrystalline silicon layer.

10. A method for making a portion of a semiconductor device comprising the steps of:

    forming an insulating layer on a surface of a semiconductor substrate;

forming a polycrystalline silicon layer on said insulating layer;

forming a covering layer on said polycrystalline silicon layer;

selectively etching away portions of said covering layer and underlying portions of said polycrystalline silicon layer;

forming insulating sidewall spacers on remaining portions of said covering layer and underlying remaining portions of said polycrystalline silicon layer, leaving an exposed portion of said insulating layer;

etching away said exposed portion of said insulating layer, leaving exposed for further processing active areas of said semiconductor substrate;

electrically connecting said polycrystalline silicon layer to said semiconductor substrate with an ohmic connection; and

connecting said polycrystalline silicon layer to an electric potential selected to prevent current flow between said active areas.

11. The method described in claim 10 wherein said polycrystalline silicon layer is electrically connected to said substrate by a metal silicide local interconnect.

12. A method for making a portion of a semiconductor device comprising the steps of:

forming a first insulating layer on a surface of a semiconductor substrate;

forming a first polycrystalline silicon layer on said first insulating layer;

forming a covering layer on said polycrystalline silicon layer,

selectively etching away portions of said covering layer and underlying portions of said first polycrystalline silicon layer;

forming a first set of insulating sidewall spacers on remaining portions of said covering layer and underlying remaining portions of said first polycrystalline silicon layer, leaving an exposed portion of said first insulating layer;

etching away said exposed portion of said first insulating layer, leaving exposed active areas of said semiconductor substrate;

forming a second insulating layer on said active areas of said semiconductor substrate;

forming a second polycrystalline silicon layer on said second insulating layer;

forming a metal silicide layer on said second polycrystalline silicon layer;

selectively etching away portions of said metal silicide layer, underlying portions of said second polycrystalline silicon layer and underlying portions of said second insulating layer;

forming lightly doped drain and source extensions;

forming a second set of insulating sidewall spacers on remaining portions of said metal silicide layer, underlying remaining portions of said second polycrystalline silicon layer and underlying remaining portions of said second insulating layer;

forming heavily doped drain and source regions;

electrically connecting said first polycrystalline silicon layer to said semiconductor substrate with an ohmic connection;

electrically connecting one or more of said source regions to said semiconductor substrate; and

connecting said first polycrystalline silicon layer to an electric potential selected to prevent current flow between said active areas.

13. The method described in claim 12 wherein said semiconductor substrate is connected to said one or more of said source regions by a metal silicide local interconnect.

14. A method for making a portion of a semiconductor device comprising the steps of:

forming a first insulating layer on a surface of a semiconductor substrate;

forming a first polycrystalline silicon layer on said first insulating layer;

forming a covering layer on said polycrystalline silicon layer;

selectively etching away portions of said covering layer and underlying portions of said first polycrystalline silicon layer;

forming a first set of insulating sidewall spacers on remaining portions of said covering layer and underlying remaining portions of said first polycrystalline silicon layer, leaving an exposed portion of said first insulating layer;

etching away said exposed portion of said first insulating layer, leaving exposed active areas of said semiconductor substrate;

forming a second insulating layer on said active areas of said semiconductor substrate;

forming a second polycrystalline silicon layer on said second insulating layer;

forming a metal silicide layer on said second polycrystalline silicon layer;

selectively etching away portions of said metal silicide layer, underlying portions of said second polycrystalline silicon layer and underlying portions of said second insulating layer;

forming lightly doped drain and source extensions;

forming a second set of insulating sidewall spacers on remaining portions of said metal silicide layer, underlying remaining portions of said second polycrystalline silicon layer and underlying remaining portions of said second insulating layer;

forming heavily doped drain and source regions;

electrically connecting said first polycrystalline silicon layer to said semiconductor substrate with an ohmic connection.

electrically connecting one or more of said drain regions to said semiconductor substrate; and

connecting said first polycrystalline silicon layer to an electric potential selected to prevent current flow between said active areas.

**15.** The method described in any one of claims 10, 12 or 14, wherein said first insulating layer has openings and said first polycrystalline silicon layer fills said openings to make a buried direct contact with said semiconductor substrate

**16.** The method described in claim 14 wherein said semiconductor substrate is connected to said one or more of said drain regions by a metal silicide local interconnect.

**17.** A method for making a memory array portion and peripheral circuit portion of a semiconductor device, comprising the steps of:

forming a blanket nitride mask layer over a memory portion of a semiconductor substrate;

forming a peripheral nitride mask layer over a peripheral portion of said semiconductor substrate;

selectively etching said peripheral nitride mask layer, leaving exposed regions of said peripheral portion of said semiconductor substrate;

growing a field oxide on said exposed regions of said peripheral portion of said semiconductor substrate;

removing said blanket nitride mask layer and remaining portions of said peripheral nitride mask layer;

forming an insulating layer on said memory portion of said semiconductor substrate;

forming a polycrystalline silicon layer on said insulating layer;

forming a covering layer on said polycrystalline silicon layer;

selectively etching away portions of said covering layer and underlying portions of said polycrystalline silicon layer;

forming insulating sidewall spacers on remaining portions of said covering layer and underlying remaining portions of said polycrystalline silicon layer, leaving an exposed portion of said insulating layer;

etching away said exposed portion of said insulating layer, leaving exposed for further processing active areas of said memory portion of said semiconductor substrate;

electrically connecting said polycrystalline silicon layer to said semiconductor substrate with an ohmic connection; and

connecting said polycrystalline silicon layer to an electric potential selected to prevent current

flow between said active areas.

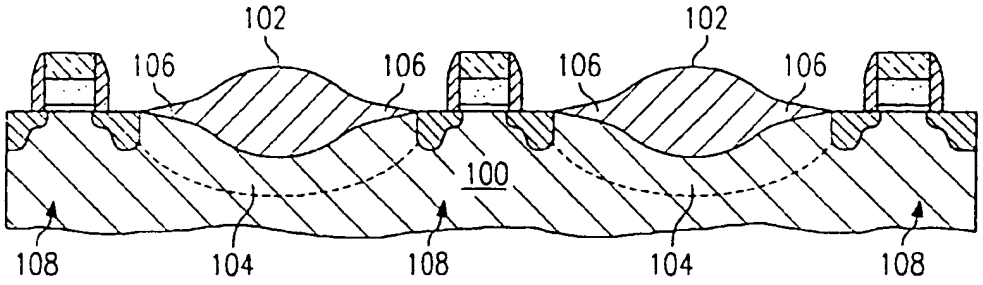



*FIG. 1*
*(PRIOR ART)*

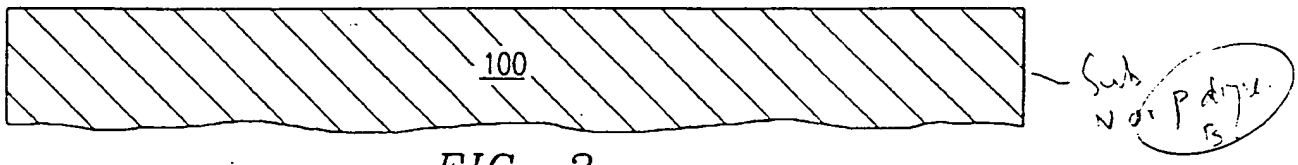



*FIG. 2*

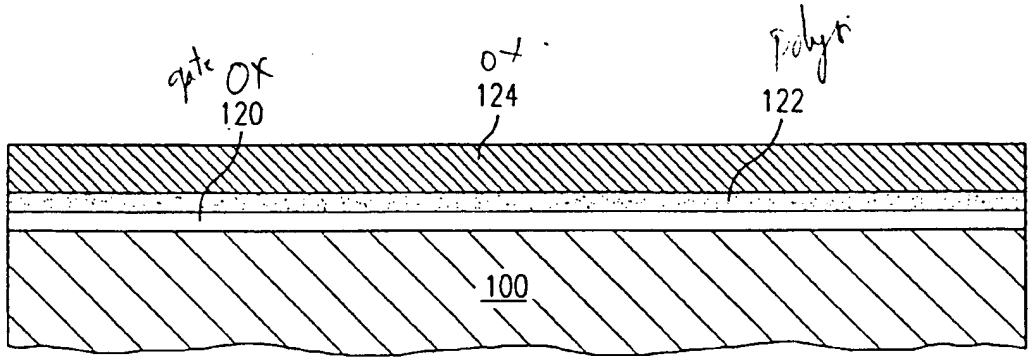



*FIG. 3*

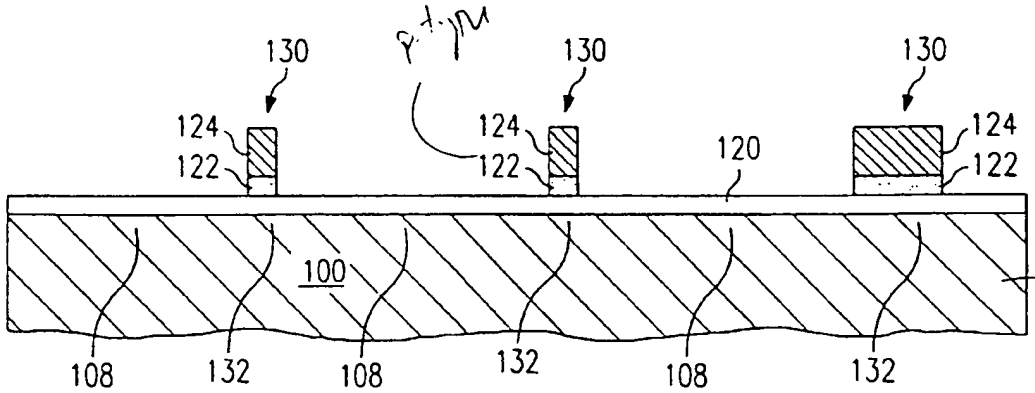



*FIG. 4*

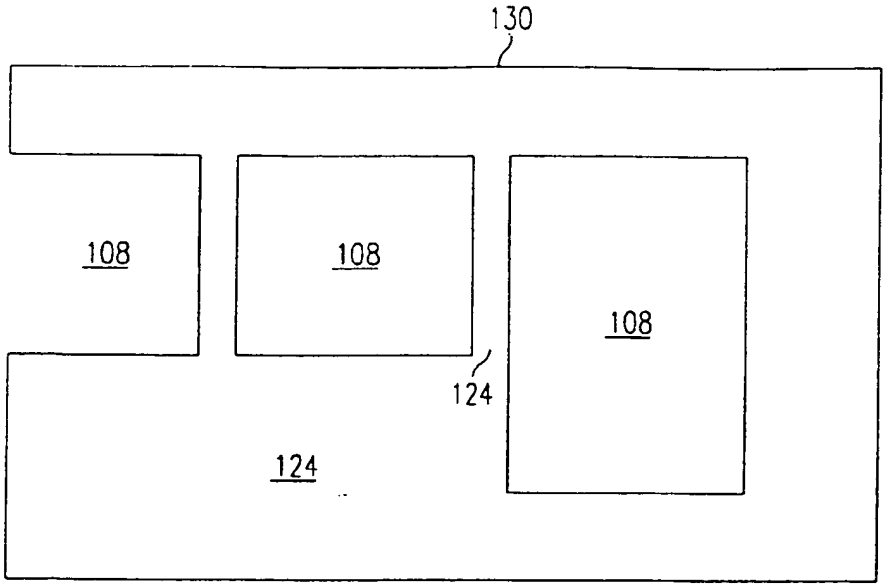



FIG. 5

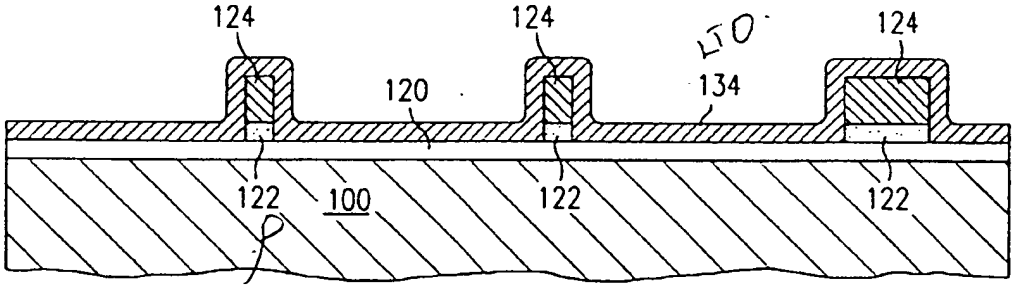



FIG. 6

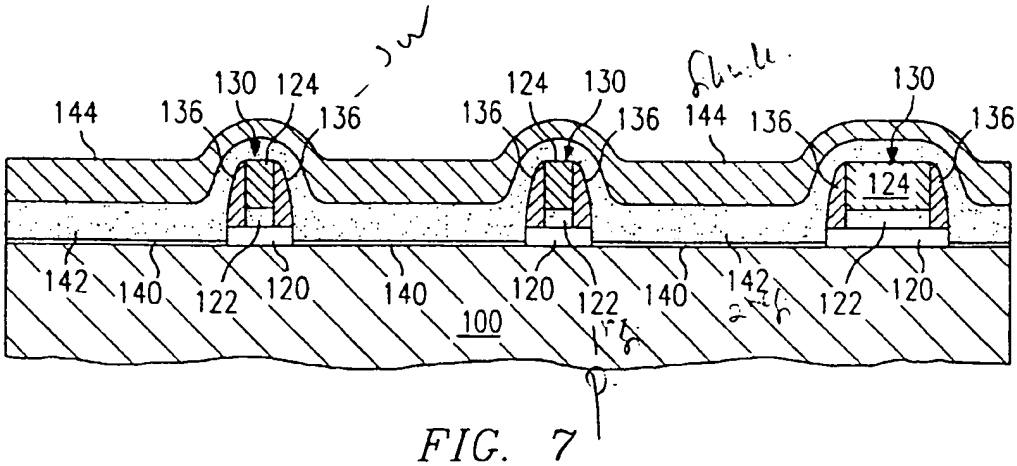



FIG. 7

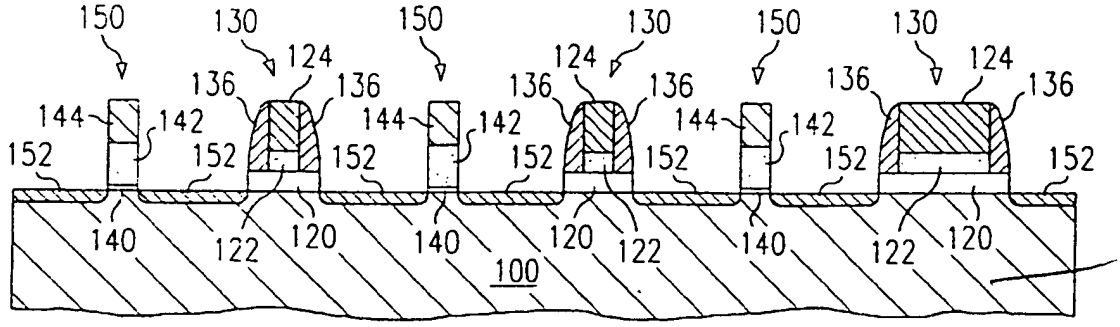



FIG. 8

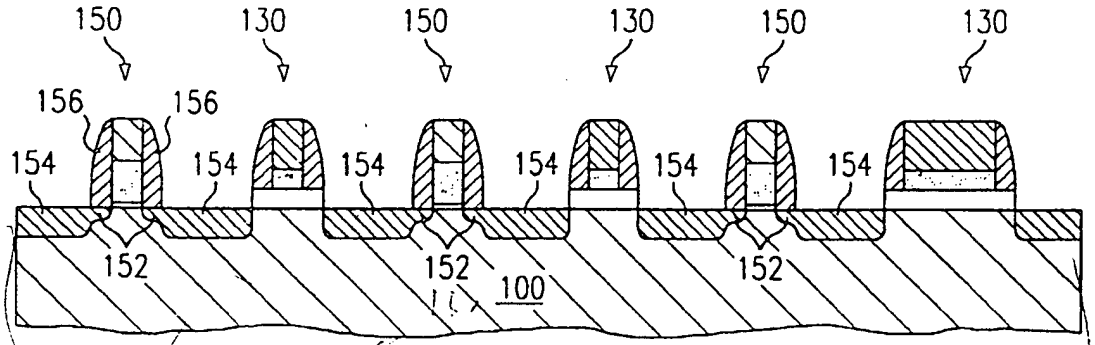



FIG. 9

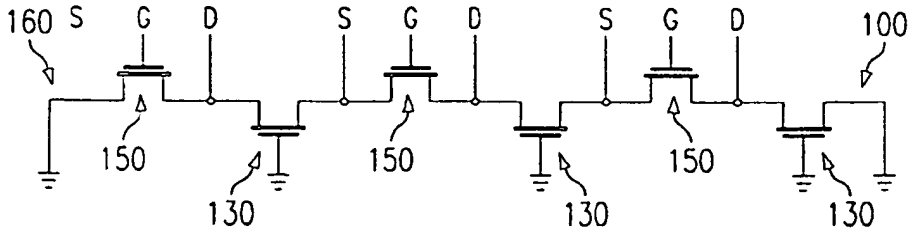
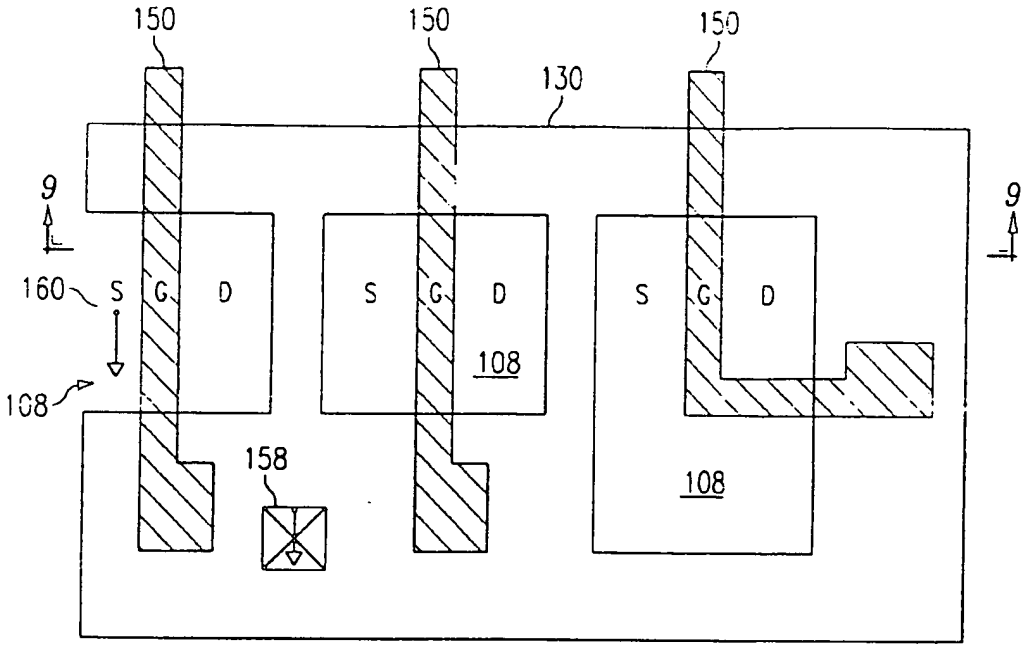



FIG. 10


150
150
150
130
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108
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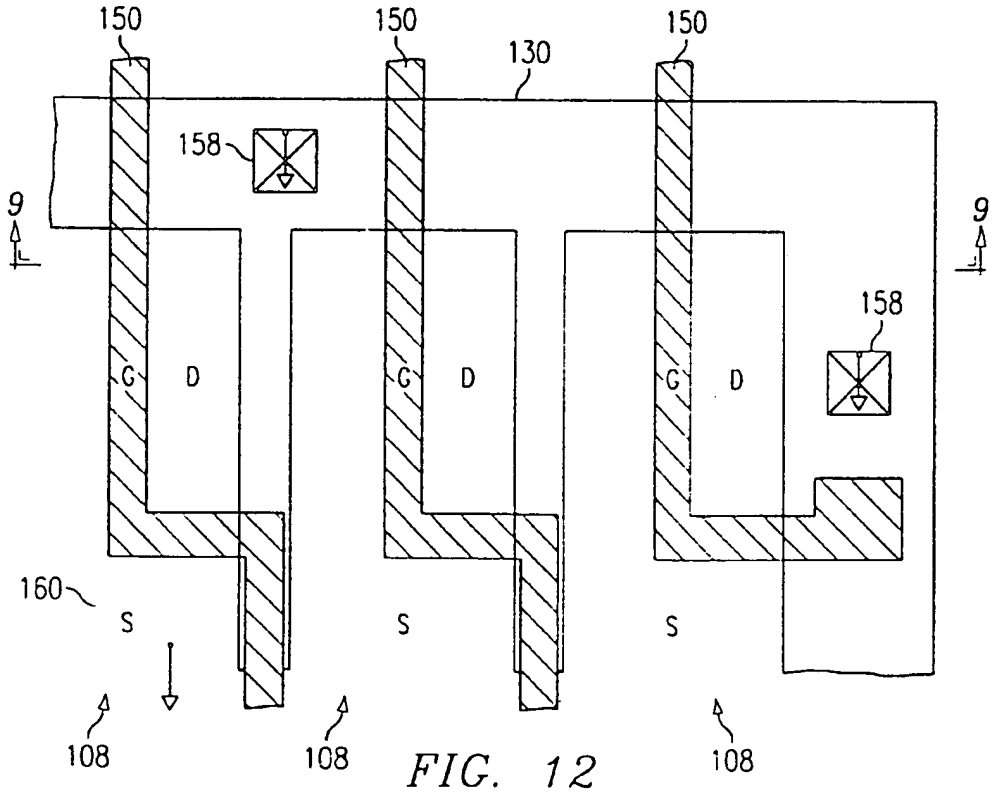
158
108

FIG. 11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108

FIG. 12